IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **ARMILLI ET AL.**	§	Attorney Docket No. **AUS920020194US1**
Serial No.: **10/733,953**	§	Examiner: **RUIZ, ARACELIS**
Filed: **10 DECEMBER 2003**	§	Art Unit: **2189**
For: **MEMORY SPECULATION IN A MEMORY SUBSYSTEM OF A DATA PROCESSING SYSTEM**	§	Confirmation No.: **8162**

APPEAL BRIEF UNDER 37 C.F.R. 41.37

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Sir:

This Appeal Brief is submitted in support of the Appeal of the Examiner's final rejection of Claims 1-6 and 8-24 in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest in the present Appeal is International Business Machines Corporation, the Assignee of the present application.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending Appeal.

STATUS OF CLAIMS

Claims 1-18 were originally presented. During prosecution, Claims 19-24 were entered, and Claim 7 was canceled. Claims 1-6 and 8-24, which comprise all pending claims, stand finally rejected by the Examiner as noted in the Final Office Action dated March 4, 2010. The rejection of each of Claims 1-6 and 8-24 is appealed.

STATUS OF AMENDMENTS

No amendments to the claims have been proposed or entered subsequent to the Final Office Action that led to this appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

Exemplary independent Claim 1 recites a data processing system including a system memory, a plurality of processing cores, and a plurality of a cache memories each coupled to a respective one of the plurality of processing cores and to an interconnect (see, e.g., Figure 1, data processing system 8; page 6, line 1 though page 7, line 2). The plurality of cache memories temporarily hold cache lines of data identified by addresses of storage locations in the system memory and certain of the plurality of cache memories service memory access requests received via the interconnect that target those addresses (see, e.g., page 6, lines 13-24). A memory controller, coupled to the interconnect and to the system memory, controls access to the system memory (see, e.g., Figure 1, IMC 18; page 6, lines 25-28). The memory controller having a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing the system memory (see, e.g., Figure 1, MST 20; col. 9,

lines 21 though page 11, line 20). Responsive to receipt of a memory access request specifying a target system memory address that is broadcast to the memory controller and the plurality of cache memories, the memory controller speculatively initiates access to the system memory to service the memory access request in advance of receipt of a coherency message indicating whether or not the memory access request is to be serviced by the memory controller accessing the system memory if speculative access is indicated by the memory speculation mechanism (see, e.g., Figure 5A, blocks 108, 110 and 120; page 14, lines 25-29). If speculative access is not indicated by the memory speculation mechanism, the memory controller initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory (see, e.g., Figure 5A, blocks 108-114; page 14, lines 12-24).

In addition to the features of underlying independent Claim 1, dependent Claim 3 recites that the memory speculation mechanism includes a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within the one or more processing cores (see, e.g., Figure 3, MST 20; page 10, lines 1-6).

In addition to the features of underlying independent Claim 1, dependent Claim 4 recites that the system memory includes a plurality of storage locations arranged in a plurality of banks and that the memory speculation mechanism stores the historical information on a per-bank basis (see, e.g., Figure 1, banks 28a, 28b; Figure 3, timing speculation fields 84; page 10, lines 7-8).

In addition to the features of underlying independent Claim 1, dependent Claim 6 recites that the data processing system includes a first system memory, first memory controller, second system memory, and second memory controller (see, e.g., Figure 1; system memories 22a, 22n and associated IMCs). The first memory controller speculatively initiates access to the first system memory based upon historical information recorded by the second memory controller (see, e.g., Figure 7; page 19, lines 7-24).

Independent Claim 9 recites a memory controller for controlling access to a system

memory of a data processing system (see, e.g., Figure 1, IMC 18 of data processing system 8; page 6, line 1 though page 7, line 2). The memory controller includes a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing the system memory (see, e.g., Figure 1, MST 20; col. 9, lines 21 though page 11, line 20). Responsive to receipt of a memory access request broadcast to the memory controller and a plurality of cache memories in the data processing system, control logic in the memory controller speculatively initiates access to the system memory to service the memory access request in advance of receipt of a coherency message indicating whether or not the memory access request is to be serviced by the memory controller accessing the system memory if speculative access is indicated by the memory speculation mechanism (see, e.g., Figure 5A, blocks 108, 110 and 120; page 14, lines 25-29). If speculative access is not indicated by the memory speculation mechanism, the control logic initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory (see, e.g., Figure 5A, blocks 108-114; page 14, lines 12-24).

In addition to the features of underlying independent Claim 9, dependent Claim 10 recites that the memory speculation mechanism includes a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within the one or more processing cores (see, e.g., Figure 3, MST 20; page 10, lines 1-6).

In addition to the features of underlying independent Claim 9, dependent Claim 11 recites that the system memory includes a plurality of storage locations arranged in a plurality of banks and that the memory speculation mechanism stores the historical information on a per-bank basis (see, e.g., Figure 1, banks 28a, 28b; Figure 3, timing speculation fields 84; page 10, lines 7-8).

In addition to the features of underlying independent Claim 9, dependent Claim 13 recites that the control logic speculatively initiates access to the system memory based upon historical information recorded by another memory controller of another system memory (see, e.g., Figure 7; page 19, lines 7-24).

Independent Claim 14 recites a method of operating a memory controller for a system memory of a data processing system (see, e.g., Figure 1, IMC 18 of data processing system 8; page 6, line 1 though page 7, line 2). According to the method, the memory controller stores, in a memory speculation mechanism, historical information regarding whether or not prior memory accesses were serviced by access to the system memory (see, e.g., Figure 1, MST 20; col. 9, lines 21 though page 11, line 20). In response to a memory access request specifying a target system memory address, if speculative access is indicated by the memory speculation mechanism, the memory controller speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not the memory access request is to be serviced by the memory controller accessing the system memory (see, e.g., Figure 5A, blocks 108, 110 and 120; page 14, lines 25-29). If speculative access is not indicated by the memory speculation mechanism, the memory controller initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory (see, e.g., Figure 5A, blocks 108-114; page 14, lines 12-24).

In addition to the features of underlying independent Claim 14, dependent Claim 15 recites that the storing step includes stores a respective memory access history for each of a plurality of threads executing within the one or more processing cores (see, e.g., Figure 3, MST 20; page 10, lines 1-6).

In addition to the features of underlying independent Claim 14, dependent Claim 16 recites that the system memory includes a plurality of storage locations arranged in a plurality of banks and that the storing comprises storing the historical information within the memory speculation table on a per-bank basis (see, e.g., Figure 1, banks 28a, 28b; Figure 3, timing speculation fields 84; page 10, lines 7-8).

In addition to the features of underlying independent Claim 14, dependent Claim 18 recites that the step of speculatively initiating access includes speculatively initiating access to

the system memory based upon historical information recorded by another memory controller of another system memory (see, e.g., Figure 7; page 19, lines 7-24).

In addition to the features of underlying independent Claim 1, dependent Claim 19 recites that the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message (see, e.g., Figure 5A, block 134; page 15, lines 1-8).

In addition to the features of underlying independent Claim 1, dependent Claim 20 recites that the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request (see, e.g., Figure 5A, block 130; page 15, lines 1-8).

In addition to the features of underlying independent Claim 9, dependent Claim 21 recites that the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message (see, e.g., Figure 5A, block 130; page 15, lines 1-8).

In addition to the features of underlying independent Claim 9, dependent Claim 22 recites that the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request (see, e.g., Figure 5A, block 130; page 15, lines 1-8).

In addition to the features of underlying independent Claim 14, dependent Claim 23 recites that the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message (see, e.g., Figure 5A, block 134; page 15, lines 1-8).

In addition to the features of underlying independent Claim 14, dependent Claim 24 recites that the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request (see, e.g., Figure 5A, block 130; page 15, lines 1-8).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are:

I. the final rejection of Claims 1-4, 6, 8-11, 13-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,697,919 B1 to *Gharachorloo et al.* (*Gharachorloo*) in view of U.S. Patent Publication No. 2002/0178349 A1 to *Shibayama et al.* (*Shibayama*)

> (The resolution of this ground of rejection will also be determinative of the final rejection of Claims 5, 12 and 17 under 35 U.S.C. § 103(a) as unpatentable over *Gharachorloo* and *Shibayama* in view of U.S. Patent Publication No. 2003/0154351 A1 to *Nilsson et al.*);

II. the final rejection of Claims 19, 21 and 23 under 35 U.S.C. § 103(a) as unpatentable over *Gharachorloo* and *Shibayama* in view of U.S. Patent Publication No. 2003/0033510 A1 to *Dice*

> (It should be noted that the Final Office Action has a typographical error and incorrectly identifies the claims rejected on this ground as Claims 19, 21 and 13); and

III. the final rejection of Claims 20, 22 and 24 under 35 U.S.C. § 103(a) as unpatentable over *Gharachorloo* and *Shibayama* in view of U.S. Patent No. 5,926,831 to *Revilla et al.* (*Revilla*).

ARGUMENT

I. Rejection of Claims 1-4, 6, 8-11, 13-16 and 18 under 35 U.S.C. § 103(a)

Claims 1-4, 6, 8-11, 13-16 and 18 stand finally rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,697,919 to *Gharachorloo* in view of U.S. Patent Publication No. 2002/0178349 to *Shibayama* (Final Office Action, page 2). That rejection is not well founded and should be reversed because it does not satisfy the legal requirements for a finding of obviousness under 35 U.S.C. § 103.

As set forth in MPEP 2141:

> As reiterated by the Supreme Court in *KSR*, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:
>
> (A) Ascertaining the scope and content of the prior art; and
> (B) Ascertaining the differences between the claimed invention and the prior art; and
> (C) Resolving the level of ordinary skill in the pertinent art.

Further, "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), 82 USPQ2d 1385, 1396.

A. Exemplary Independent Claim 1

1. Combination of *Gharachorloo* and *Shibayama* does not disclose the "memory controller" recited in exemplary independent Claim 1

The combination of *Gharachorloo* and *Shibayama* does not render exemplary independent Claim 1 unpatentable under 35 U.S.C. § 103(a) because that combination of references does not disclose or render obvious each feature recited therein, and in particular, does not disclose or render obvious a "memory controller" having a memory speculative mechanism as recited in exemplary Claim 1 as follows:

> a memory controller … having a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing the system memory.

a. Scope and content of the prior art

At correctly noted by the Examiner at page 3 of the Final Office Action, *Gharachorloo* "does not teach said memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the

system memory." The Examiner therefore relies upon paragraphs [0062] and [0064] of *Shibayama* as disclosing the claimed memory controller (Final Office Action, pages 3-4).

The cited paragraphs of *Shibayama* and the remainder of that reference disclose a processor including a data dependence speculation control device 10 that controls speculative execution of a memory access instruction out-of-order with respect to preceding instructions on which the memory access instruction may be data-dependent by reference to a speculative execution result history table 12 that indicates whether previous speculative (out-of-order) executions of the memory access instruction were successful or failures (*Shibayama*, Abstract and Figure 3). Thus, *Shibayama's* disclosure is directed to a processor's speculative instruction execution based upon historical information indicating whether or not prior speculative (out-of-order) executions of a memory access instruction have correctly observed data-dependencies, if any, on other memory access instructions (see, e.g., *Shibayama*, Figure 12) rather than a memory controller's speculative access to system memory based upon whether or not prior memory accesses were serviced by accessing the system memory as claimed.

b. Differences between the claimed invention and the prior art

When *Gharachorloo* and *Shibayama* are combined without reference to the teachings of the present application, that combination discloses a multiprocessor data processing system as taught by *Gharachorloo* in which individual CPUs employ out-of-order speculative execution of memory access instructions by reference to the success or failure of prior out-of-order executions in observing data-dependencies as disclosed by *Shibayama*. As should be apparent, such a combination of references fails to disclose each feature recited in exemplary Claim 1, and specifically fails to disclose or render obvious the claimed memory controller "having a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing the system memory."

It should be noted that the Examiner in the Final Office Action incorrectly assumes without discussion that the combination of *Gharachorloo* and *Shibayama* yields the invention recited in Claim 1. Consequently, the Examiner does not acknowledge the divergence of the

combined teaching of *Gharachorloo* and *Shibayama* from the claimed subject matter, and therefore fails to provide any reasoning supporting modifications to the reference teachings to obtain the claimed subject matter. For example, at page 3 of the present Office Action, the Examiner asserts without any citation to the references that "Shibayama et al. teaches said memory controller …." However, *Shibayama* fails to disclose a memory controller at all and instead discloses a processor core (see, e.g., *Shibayama*, paragraph [0105]). Further, at page 3 of the Office Action, the Examiner asserts that the success or failure indications provided by *Shibayama's* speculative execution result history table 12 disclose the claimed "historical information regarding whether or not prior memory accesses were serviced by accessing the system memory." However, when the reference teachings are actually examined, it is clear that *Shibayama's* success/failure indications predict, based upon prior executions, whether or not a potentially data-dependent memory access instruction can be executed out-of-order without a data-dependency requiring a recovery operation and in-order execution (see, e.g., *Shibayama*, Abstract). *Shibayama's* success/failure indications provide no information "regarding whether or not prior memory accesses were serviced by accessing the system memory," as claimed.

c. Claim 1 is not obvious in view of the combination of references

Because the Examiner has mischaracterized the reference teachings and failed to note the differences between the claimed invention and the prior art, the Examiner has clearly failed to satisfy the requirements for a determination of obviousness enunciated by *Graham v. John Deere Co.*, 383 U.S. 1 (1966). Consequently, the final rejection of exemplary Claim 1, similar Claims 9 and 14 and their respective dependent claims under 35 U.S.C. § 103 in view of *Gharachorloo* and *Shibayama* should be reversed.

2. Combination of *Gharachorloo* and *Shibayama* does not disclose the timing speculation recited in exemplary independent Claim 1

The rejection of exemplary independent Claim 1 under 35 U.S.C. § 103 in view of *Gharachorloo* and *Shibayama* should also be reversed because the combination of cited references does not disclose or render obvious different timings of access to system memory relative to a coherency message based upon a memory speculation mechanism, as claimed. In other words, the combination of cited references does not disclose speculatively accessing

system memory before a coherency message is received if the memory speculation mechanism indicates a speculative access and non-speculatively accessing system memory after a coherency message is received if the memory speculation mechanism indicates a non-speculative access, as required by the following language of Claim 1:

> … wherein said memory controller ... :
>
> if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory … in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and
>
> if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory … only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

In fact, the combination of cited references does not disclose (and the Examiner does not cite any portion of the reference as disclosing) the claimed "coherency message." Consequently, the combination of references cannot disclose or render obvious the claimed timing speculation relative to receipt of such a coherency mechanism.

In view of the manifest failure of the combination of cited references to disclose or render obvious each feature of exemplary Claim 1, the rejection of exemplary Claim 1, similar Claims 9 and 14, and their respective dependent claims under 35 U.S.C. § 103 should be reversed.

B. Combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary dependent Claim 3

The combination of *Gharachorloo* and *Shibayama* also does not render exemplary Claim 3 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 3:

> … said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

At page 9 of the Final Office Action, the Examiner relies upon *Gharachorloo's*

disclosure of a cache directory 180, instruction-level parallelism, simultaneous multithreading (SMT), and out-of-order execution as teaching the features of Claim 3. Appellants respectfully traverse the Examiner's position because none of these features of *Gharachorloo's* processor cores discloses a memory speculation table of a memory controller that stores a per-thread history, as required by the recitation that the "memory speculation table stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores." Instead, the combination of *Gharachorloo* and *Shibayama* discloses that entries in a speculative execution result history table are indexed by hashed target addresses of the memory access instructions, rather than on a per-thread basis as claimed (*Shibayama*, Abstract).

Because the combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary Claim 3, the rejection of exemplary Claim 3 and similar Claims 10 and 15 under 35 U.S.C. § 103 should be reversed.

C. Combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary dependent Claim 4

The combination of *Gharachorloo* and *Shibayama* also does not render exemplary Claim 4 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 4:

> … said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

At page 9 of the Final Office Action, the Examiner relies, *inter alia*, upon *Gharachorloo's* disclosure of memory banks as teaching the features of Claim 4. Appellants respectfully traverse the Examiner's position because *Gharachorloo's* disclosure of memory banks does not disclose a memory speculation table of a memory controller that stores a per-bank history, as required by Claim 4. Instead, the combination of *Gharachorloo* and *Shibayama* discloses that entries in a speculative execution result history table are indexed by hashed target addresses of the memory access instructions, rather than on a per-bank basis as claimed

(*Shibayama*, Abstract).

Because the combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary Claim 4, the rejection of exemplary Claim 4 and similar Claims 11 and 16 under 35 U.S.C. § 103 should be reversed.

D. Combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary dependent Claim 6

The combination of *Gharachorloo* and *Shibayama* also does not render exemplary Claim 6 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 6:

> … said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

At pages 9-10 of the Final Office Action, the Examiner relies upon *Gharachorloo's* column 21, lines 59-63 as disclosing that *Gharachorloo's* cache coherence protocol enables sharing of memory lines across multiple nodes. Appellants respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of a conventional cache coherency protocol fails to disclose or render obvious the speculative initiation of access to a system memory by a first system memory controller based upon historical information recorded by a second memory controller, as recited by Claim 6.

Because the combination of *Gharachorloo* and *Shibayama* does not disclose the features recited in exemplary Claim 6, the rejection of exemplary Claim 6 and similar Claims 13 and 18 under 35 U.S.C. § 103 should be reversed.

II. Rejection of Claims 19, 21 and 23 under 35 U.S.C. § 103(a)

Claims 19, 21 and 23 stand finally rejected under 35 U.S.C. § 103(a) as unpatentable over *Gharachorloo* and *Shibayama* in view of *Dice* (Final Office Action, page 12; note the typographical error in the Final Office Action mistakenly listing Claims 19, 21 and 13). That

rejection is also not well founded and should be reversed for the reasons set forth above with reference to exemplary Claim 1, as well as the following additional reasons.

The combination of *Gharachorloo*, *Shibayama* and *Dice* also does not render exemplary Claim 19 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features recited therein:

> … wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message. [Emphasis supplied]

With reference to these features, page 12 of the Final Office Action correctly notes, "Gharachorloo et al. and Shibayama et al. do not teach [the foregoing features of Claims 13, 19 and 21]." The Examiner then relies upon page 8 and Claim 11 of *Dice* as disclosing the claimed features. As summarized in Claim 11 of *Dice*, the combination of references discloses:

> 11. The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the step of:
>
> determining when at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory; and
>
> in response to the step of determining, the step of setting a value of a speculation indicator comprises the step of setting the value of the speculation indicator to indicate that speculative execution of instructions is allowed in the computerized device. [Emphasis supplied]

Thus, the combination of *Gharachorloo*, *Shibayama* and *Dice* discloses a system in which speculative instruction execution is allowed in response to determining "at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory." This teaching does not disclose, suggest or render obvious a condition for updating of a memory speculation mechanism, and in particular, does not disclose, suggest or render obvious updating a memory speculation mechanism in response to "confirmation of correctness of speculative access to the system memory as indicated by the coherency message," as claimed.

Because the combination of cited references does not disclose or render obvious the features recited in exemplary Claim 19, the rejection of exemplary Claim 19 and similar Claims 21 and 23 as unpatentable under 35 U.S.C. § 103 should be reversed.

III. Rejection of Claims 20, 22 and 24 under 35 U.S.C. § 103(a)

Claims 20, 22 and 24 under 35 U.S.C. § 103(a) stand finally rejected as unpatentable over *Gharachorloo* and *Shibayama* in view of *Revilla* (Final Office Action, page 12). That rejection is also not well founded and should be reversed for the reasons set forth above with reference to exemplary Claim 1. In addition, the rejection of Claims 20, 22 and 24 should be reversed because the cited combination of references does not disclose the following features recited in exemplary Claim 20:

> … wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

With reference to these features, page 13 of the Final Office Action correctly notes that the features are not taught by *Gharachorloo* or *Shibayama* and accordingly cites col. 1, lines 50-55 and col. 5, lines 47-60 of *Revilla*. The cited passages of *Revilla* disclose that for "non-well behaved" data storage, such as First-In, First-Out (FIFO) buffers, speculative access could cause the loss of data or incorrect delivery of data to a processor. *Revilla* accordingly discloses an arrangement in which a memory controller receives and services an access request (see, e.g., *Revilla*, Figure 2, block 58) and additionally conditionally performs additional speculative operation(s) only if a "guard" bit received from a processor in conjunction with the access request is not set (see, e.g., *Revilla*, Figure 2, block 64).

The combination of cited references, while disclosing that speculative access to memory should be prevented to avoid use of incorrect data, clearly does not disclose or render obvious discarding data associated with a memory access request responsive to a coherency message indicating speculative access to system was incorrect as claimed. Consequently, the combination of *Gharachorloo*, *Shibayama* and *Revilla* does not render exemplary Claim 20 and similar Claims 22 and 24 unpatentable under 35 U.S.C. § 103, and the rejection of these claims should

be reversed.

IV. Conclusion

The foregoing arguments demonstrate that the combination of cited references does not disclose each feature of Claims 1-6 and 8-24 as required to support a rejection under 35 U.S.C. § 103(a). Appellants therefore respectfully request the Board to reverse the rejection of each pending claim.

Appellants have submitted herewith the fee for the filing of a Brief in support of Appeal. A one-month extension of time fee is required at this time and should be charged to Dillon & Yudell Deposit Account No. **50-3083.** No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,

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CLAIMS APPENDIX

1. A data processing system, comprising:

a system memory;

a plurality of processing cores;

a plurality of a cache memories, each coupled to a respective one of the plurality of processing cores and to an interconnect, wherein the plurality of cache memories temporarily hold cache lines of data identified by addresses of storage locations in the system memory and certain of the plurality of cache memories service memory access requests received via the interconnect that target those addresses; and

a memory controller, coupled to said interconnect and to the system memory, that controls access to the system memory, said memory controller having a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing the system memory, wherein said memory controller, responsive to receipt of a memory access request broadcast to the memory controller and the plurality of cache memories, said memory access request specifying a target system memory address:

if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and

if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

2. The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. The data processing system of Claim 1, wherein said memory speculation mechanism

comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. The data processing system of Claim 1, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

5. The data processing system of Claim 1, wherein said coherency message comprises a combined response representing a systemwide response to said memory access request.

6. The data processing system of Claim 1, wherein:

said system memory comprises a first system memory;

said memory controller comprises a first memory controller;

said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory;

said first memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

7. (canceled)

8. The data processing system of Claim 1, and further comprising response logic that provides said coherency message for said memory access request.

9. A memory controller for controlling access to a system memory of a data processing system, said memory controller comprising:

a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon historical information regarding whether or not prior memory accesses were serviced by accessing said system memory; and

control logic that, responsive to receipt of a memory access request broadcast to the memory controller and a plurality of cache memories in the data processing system, said memory access request specifying a target system memory address:

if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and

if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

10. The memory controller of Claim 9, wherein said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of program threads executing within said data processing system.

11. The memory controller of Claim 9, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

12. The memory controller of Claim 9, wherein said coherency response comprises a combined response representing a systemwide response to said memory access request.

13. The memory controller of Claim 9, wherein said control logic speculatively initiates access to said system memory based upon historical information recorded by another memory controller of another system memory.

14. A method of operating a memory controller for a system memory of a data processing system, said method comprising:

said memory controller storing, in a memory speculation mechanism, historical information regarding whether or not prior memory accesses were serviced by access to the system memory; and

in response to a memory access request specifying a target system memory address:

if speculative access is indicated by the memory speculation mechanism, said memory controller speculatively initiating access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and

if speculative access is not indicated by the memory speculation mechanism, said memory controller initiating non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

15. The method of Claim 14, wherein said storing comprises storing a respective memory access history for each of a plurality of threads executing within said data processing system.

16. The method of Claim 14, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said storing comprises storing said historical information within said memory speculation table on a per-bank basis.

17. The method of Claim 14, wherein said coherency response comprises a combined response representing a systemwide response to the memory access request and speculatively initiating access comprises speculatively initiating access in advance of receipt by the memory controller of the combined response of said memory access request.

18. The method of Claim 14, wherein said step of speculatively initiating access comprises speculatively initiating access to said system memory based upon historical information recorded by another memory controller of another system memory.

19. The data processing system of Claim 1, wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

20. The data processing system of Claim 1, wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

21. The memory controller of Claim 9, wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

22. The memory controller of Claim 9, wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

23. The method of Claim 14, and further comprising the memory controller, responsive to the coherency message, updating the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

24. The method of Claim 14, and further comprising the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

EVIDENCE APPENDIX

none

RELATED PROCEEDINGS APPENDIX

none